

Timing Diagram

Representation of Various Control signals generated during Execution of an Instruction.

Following Buses and Control Signals must be shown in a Timing Diagram:

- Higher Order Address Bus.
- Lower Address/Data bus
- ALE
- RD
- WR
- IO/M

Timing Diagram

Instruction:

A000h MOV A,B

Corresponding Coding:

A000h 78

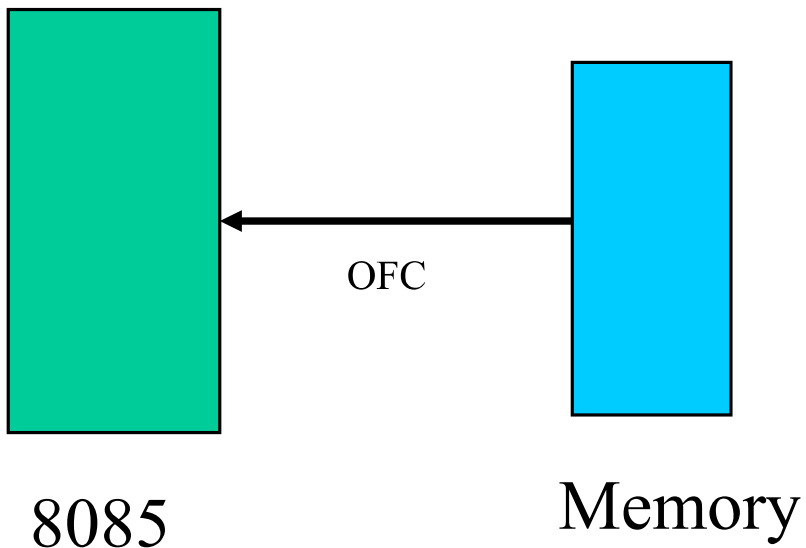
Timing Diagram

Instruction:

A000h MOV A,B

Corresponding Coding:

A000h 78



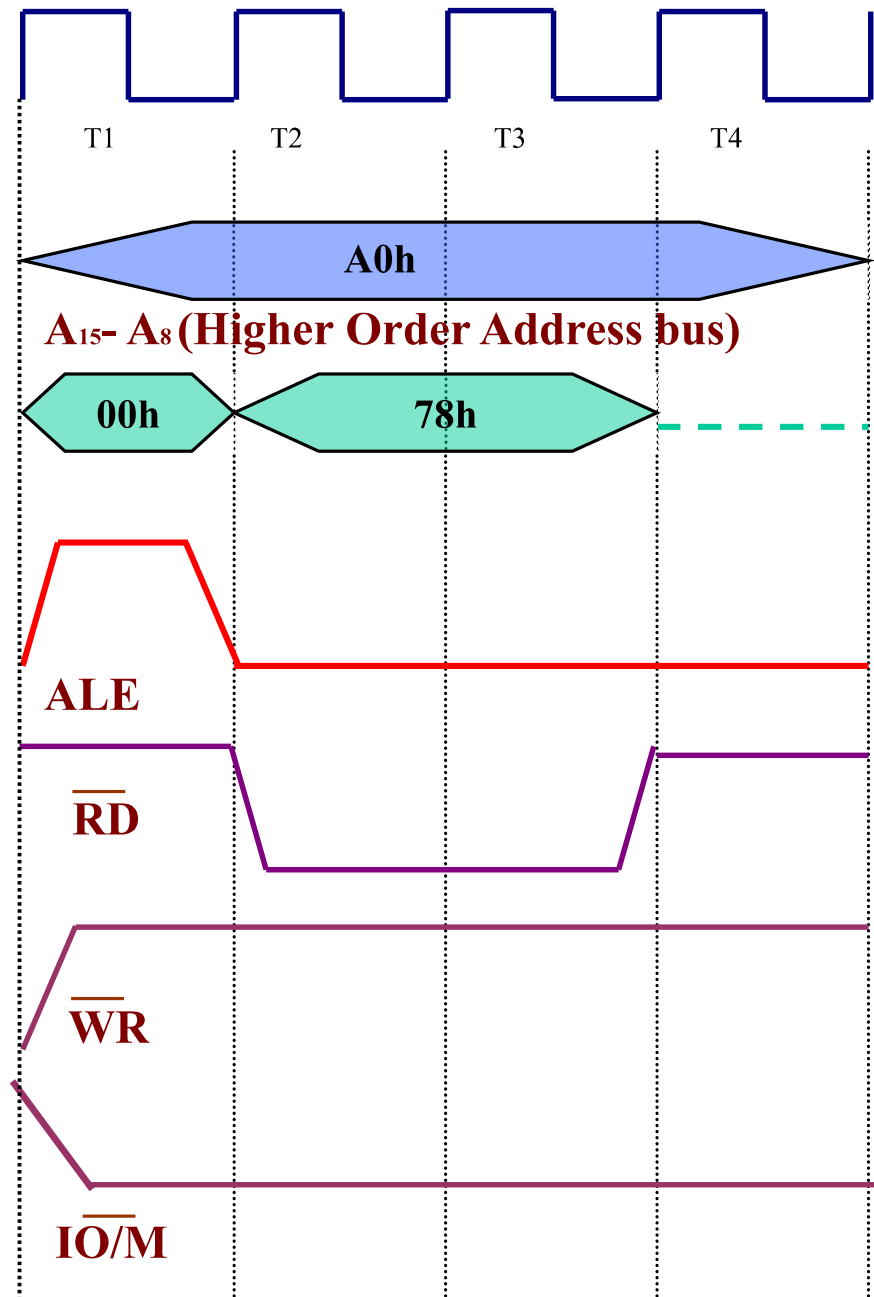
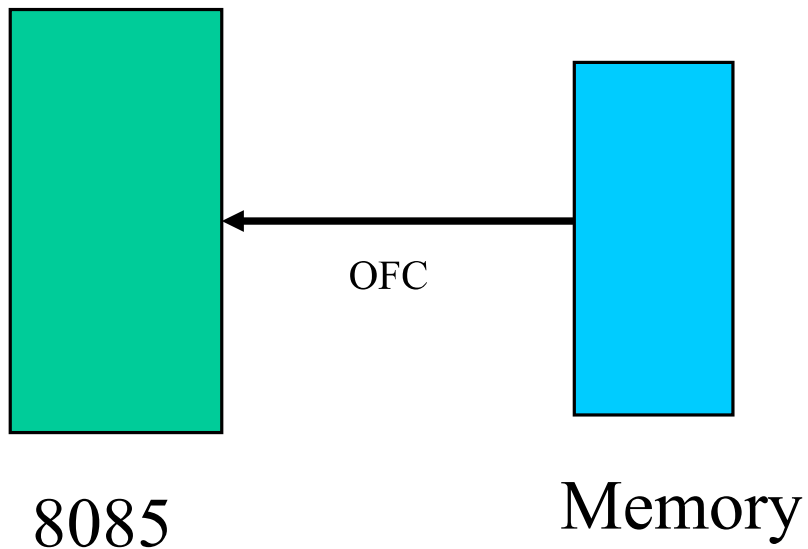
Timing Diagram

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Corresponding Coding:

A000h 78



Op-code fetch Cycle

Timing Diagram

Instruction:

A000h MVI A,45h

Corresponding Coding:

A000h 3E

A001h 45

Timing Diagram

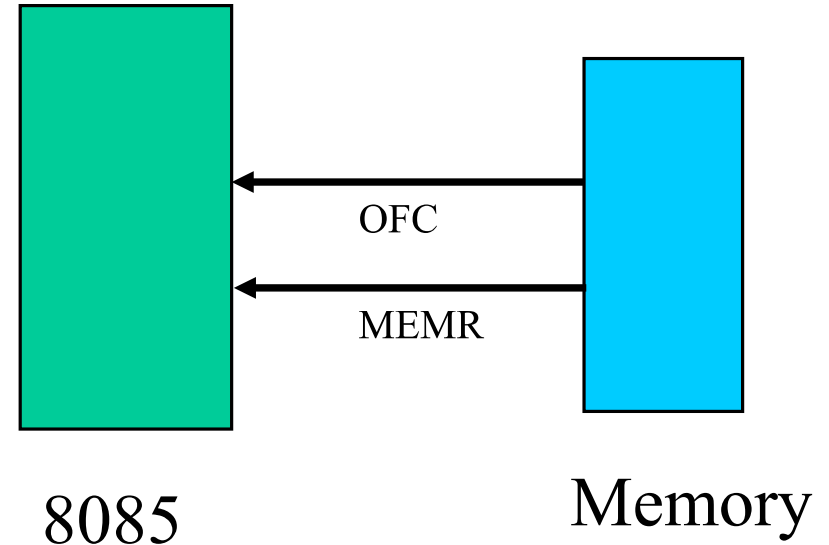
Instruction:

A000h MVI A,45h

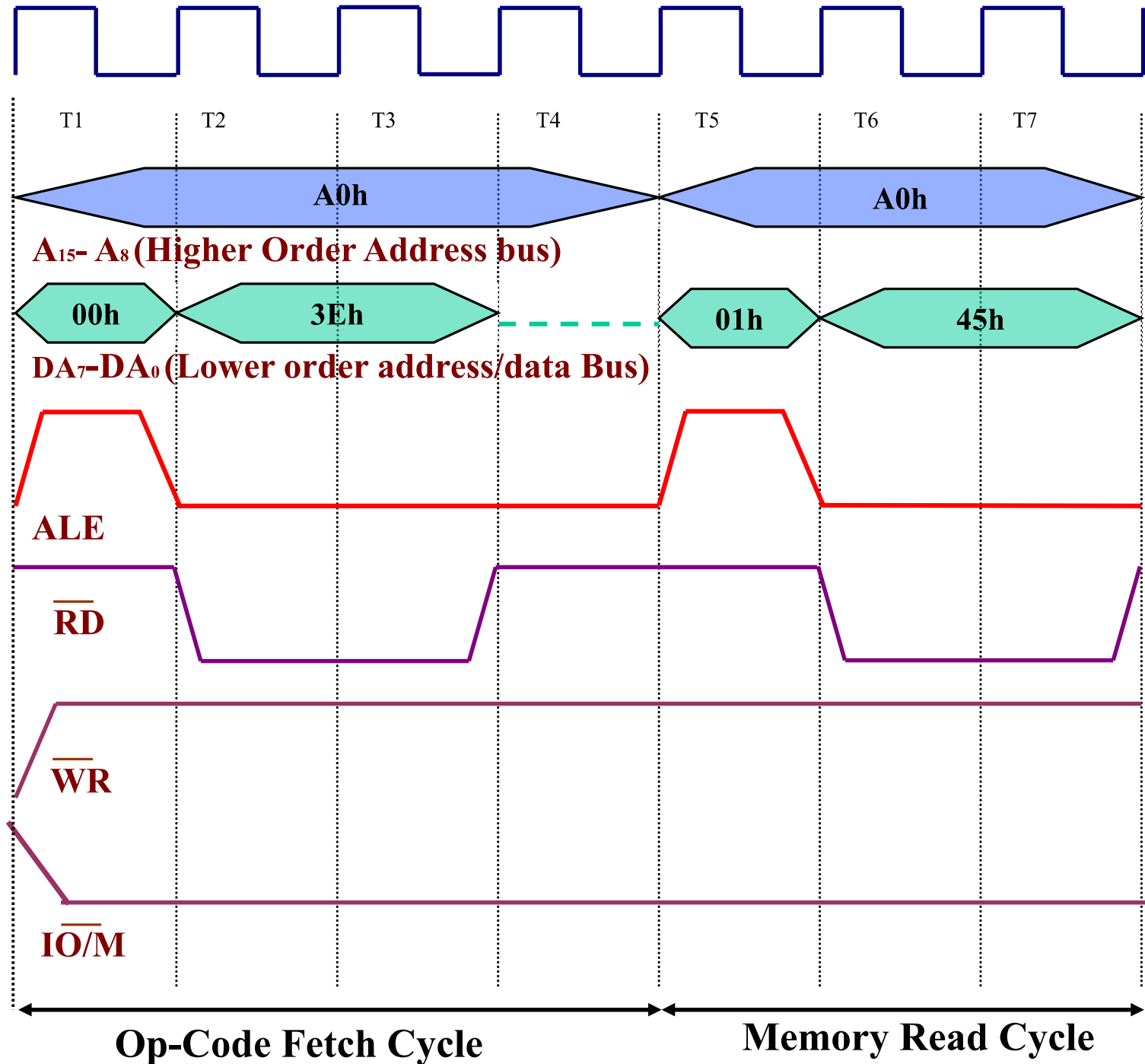
Corresponding Coding:

A000h 3E

A001h 45



Timing Diagram



Instruction:

A000h MVI A,45h

Corresponding Coding:

A000h 3E

A001h 45

Timing Diagram

Instruction:

A000h LXI A,FO45h

Corresponding Coding:

A000h 21

A001h 45

A002h F0

Timing Diagram

Instruction:

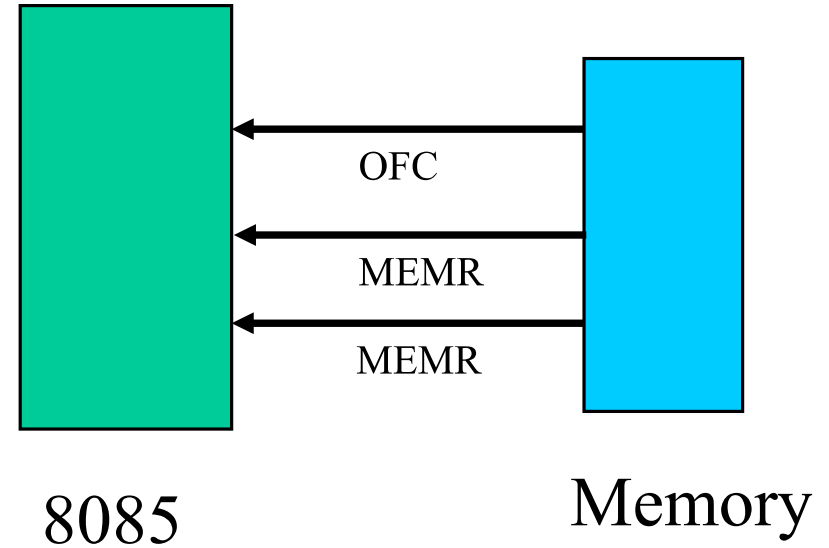
A000h LXI A,FO45h

Corresponding Coding:

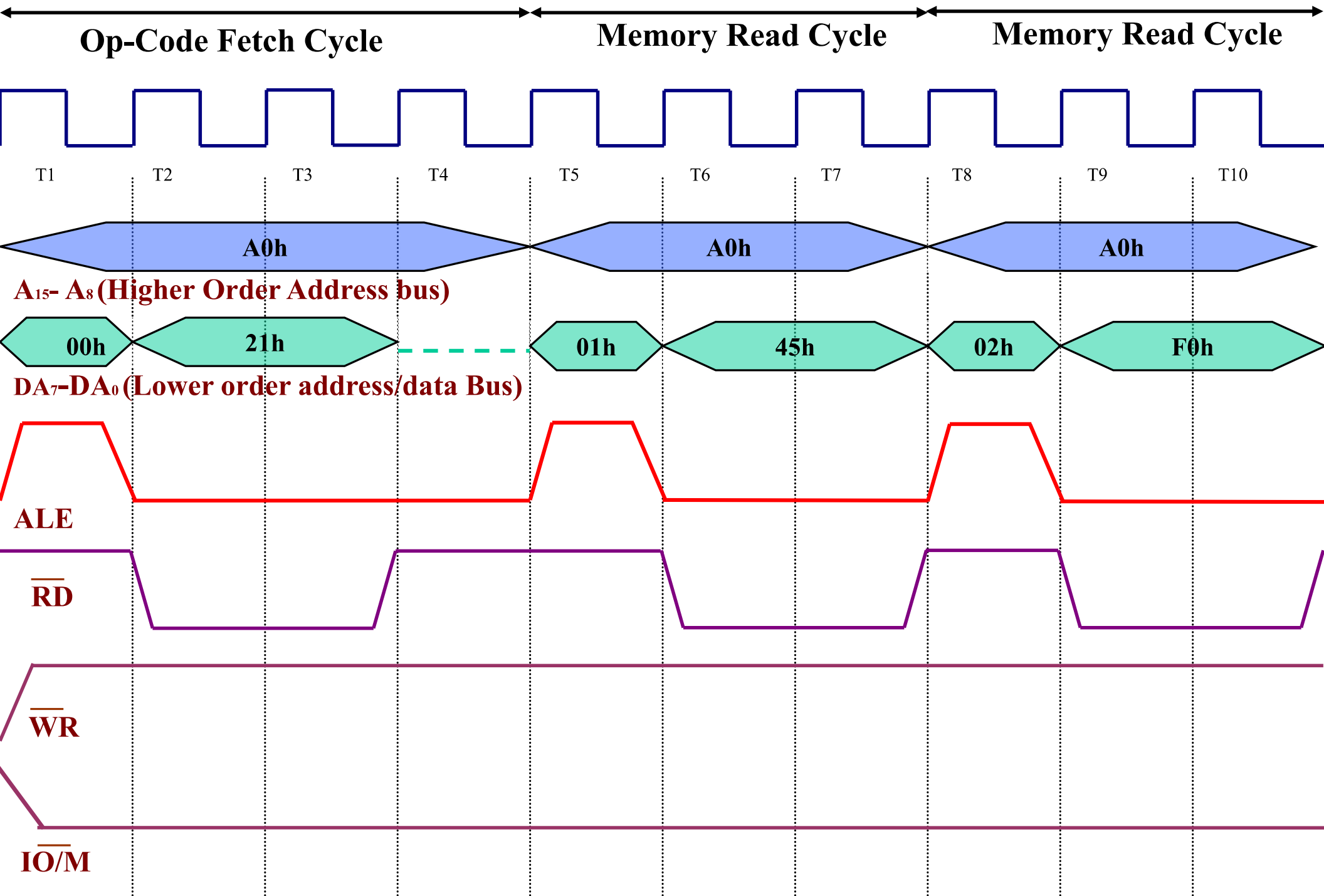
A000h 21

A001h 45

A002h F0



Timing Diagram



Timing Diagram

Instruction:

A000h MOV A,M

Corresponding Coding:

A000h 7E

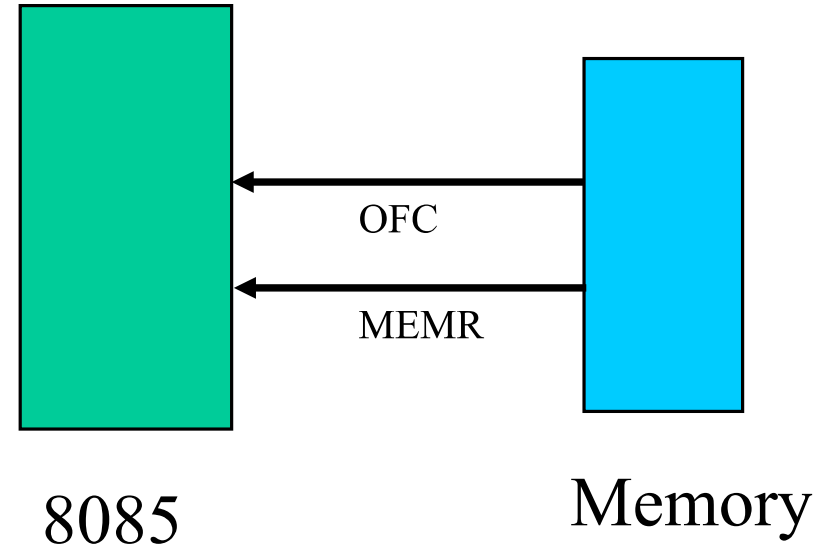
Timing Diagram

Instruction:

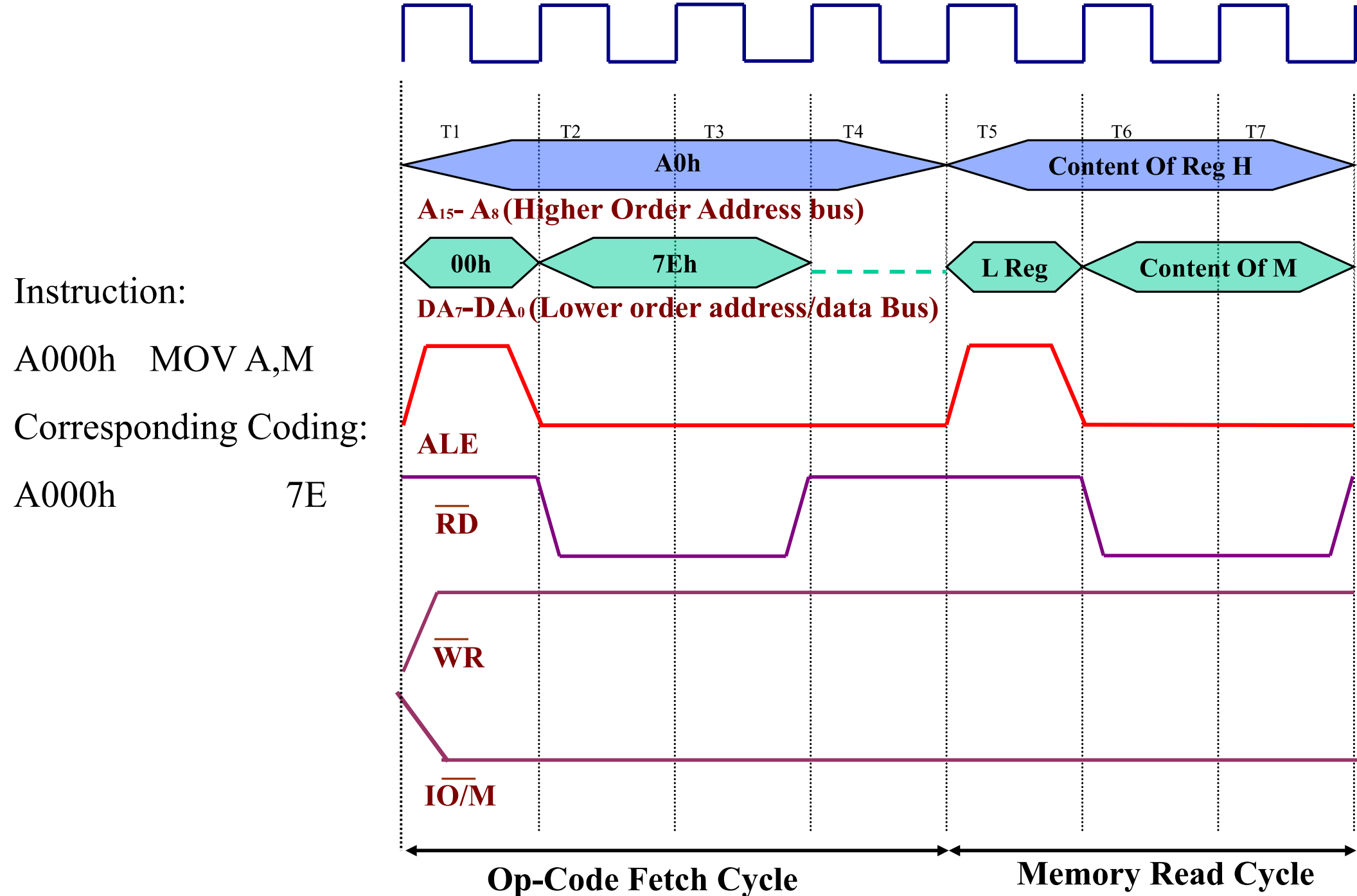
A000h MOV A,M

Corresponding Coding:

A000h 7E



Timing Diagram



Timing Diagram

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A000h MOV M,A

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A000h 77

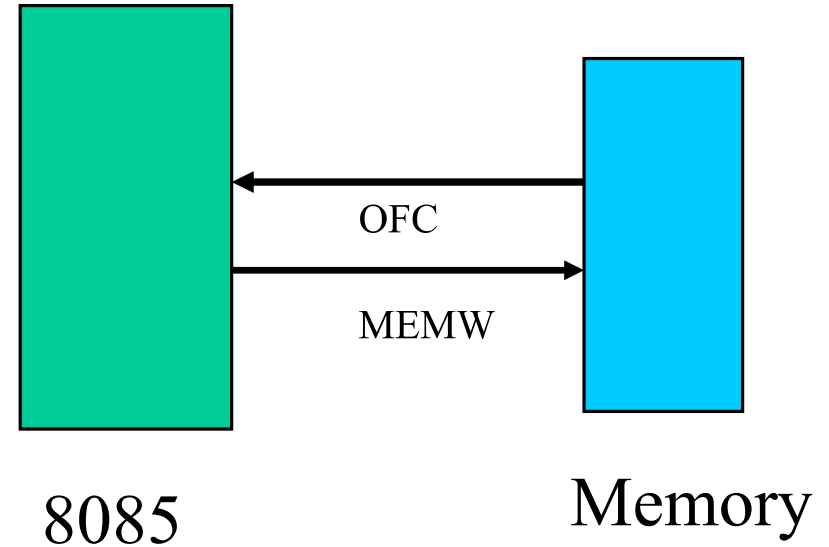
Timing Diagram

Instruction:

A000h MOV M,A

Corresponding Coding:

A000h 77



Timing Diagram

